International Journal of Power Electronics and Drive System (IJPEDS)
Vol. 11, No. 1, March 2020, pp. 515~522
ISSN: 2088-8694, DOI: 10.11591/ijpeds.v11.i1.pp515-522

Symmetrical high voltage gain half-bridge inverter based double-Y-source networks with reduced voltage stress

Hussain Sayed, Oday A. Ahmad, Dhari Y. Mahmood, Kanaan A. Jalal, Waleed H. Habeeb
Department of Electrical Engineering, University of Technology-Baghdad, Iraq

Article Info

Article history:

Received Dec 15, 2018
Revised Mar 1, 2019
Accepted Jul 8, 2019

Keywords:

Coupled inductance
Half-bridge DC-AC converter
High voltage gain inverter
Leakage inductance
Voltage stress
Y-source impedance

ABSTRACT

A single-stage symmetrical high voltage gain half-bridge (HB) DC-AC converter is proposed in this paper. Using two Y-source impedance networks, the following key features are utilized from the proposed topology: single stage inverter with very high voltage gain compared to conventional HB inverter, symmetrical output voltage waveform, low voltage stress across the passive components because it is distributed across two impedance networks, and only two switching devices are needed for the converter. Furthermore, important merit of the proposed topology is that the current drawn by the Y-coupled inductors is symmetrical around the X-axis which helps to prevent the Y-network cores from reaching the saturation state. And the last compelling feature is a virtual neutral point for the load connection is inherited in the proposed double Y-source impedance networks converter with no need for DC-Link capacitors. For low voltage sources such as photovoltaic (PV) and fuel cell, the converter is designed to achieve continuous input current operation. The operation modes and principles of the inverter are analyzed and discussed deeply in this paper. A detailed mathematical equations system is derived and verified for the presented converter. Finally, PSpice simulation tools are used to simulate the converter and verify the derived mathematical formulas.

Corresponding Author:

Hussain Sayed,
Department of Electrical Engineering,
University of Technology-Baghdad, Iraq
Alumni Member of University of Arkansas at Little Rock, Little Rock, Arkansas, United States
Email: hksayed@ualr.edu

1. INTRODUCTION

Renewable energy resources such as photovoltaic, wind turbines, and fuel cells are widely being demanded worldwide. The maximum supply voltage by those resources is low compared to AC power grid voltage standards. The output voltage also changes according to weather penetration. So that, wide range input voltage DC-AC power converters with high voltage gain are needed for clean energy applications. Conventional voltage source inverters (half and full bridge converters) are not promising topologies for renewable energy application because they have no voltage gain in basic operating principles.

High voltage gain inverters were proposed based on using different source impedance configurations as explored in next. In [1], a full-bridge single-phase inverter was proposed using Z-source impedance. The converter consists of four switching devices with a Z-source impedance to achieve high voltage gain with the discontinuous input current. Reference [2] proposed a switched-boost single phase HB inverter using two Z-source impedance networks. In addition to the voltage gain limitation of Z-source impedance inverters (the maximum output gained voltage is equal to twice its input to the Z-network), two additional DC-Link capacitors are needed for the HB converter to create a neutral point for the load connection. The voltage stress across the two capacitors is equal to twice the peak value of the output AC gained voltage, which means DC-Link capacitors with high voltage rating are required in such topology. A novel quasi-Z-source HB DC-DC converter is introduced in [3]. The proposed topology has a high-frequency transformer with a voltage doubler to obtain high voltage gain as well as circuit isolation. With Asymmetrical voltage waveform generated by the HB inverter, DC voltage component would exist in the voltage waveform. The challenges of selecting a blocking capacitor to prevent the DC component from passing through the high frequency transformer makes the converter more complicated. Otherwise, the high-frequency transformer would be exposed to the saturation problem. A single-phase high voltage gain DC-DC converter was presented for a half-bridge photovoltaic inverter system in [4]. The main disadvantage of the proposed converter is that many switching devices are required for the boost converter, resulting in low power converter reliability, and high power loss. Also, high voltage stress is experienced across the output capacitors of the proposed boost converter. An isolated transformer boost half-bridge micro-inverter for a single-phase PV system was explored in [5]. Using an isolated transformer helps to increase the voltage gain of the converter, but it increases the power conversion stages and more switching devices to achieve the required grid voltage level. In so doing that, the reliability of the converter is reduced as many components are needed to reach the grid voltage level. A Z-source inverter with high voltage gain capability is proposed in [6]. The disadvantage of this topology is that in case of failure of either one of the input power supplies (or in case of unequal voltage supply), asymmetrical output voltage waveform is expected to appear across the load. In addition to that, the extension of the proposed topology needs many components to be used to achieve the desired voltage gain. In [7], a high gain switched-boost half-bridge inverter is presented. The converter has a lower voltage gain than the proposed topology in this paper. A novel quasi-Z-source half-bridge DC-DC converter was introduced in [8]. The output AC voltage of quasi-Z-source inverter should be equal to the half value of the DC gained voltage, which is countered what is mentioned the operation waveforms of the proposed topology, according to the conventional half-bridge inverter operation. In [9], a Z-source half-bridge inverter is proposed, which requires two DC-Link capacitors with high voltage rating because the stress voltage across those capacitors are high. Although the stress voltage of the capacitors is reduced-based HB inverter, but the voltage gain is still not higher than other Y-source impedance networks converters [10]. In addition to that, the proposed topology is applicable only for two symmetrical input voltage supplies. Quasi-Z-source DC converter for high power photovoltaic applications is shown in [11]. The main drawback of the topology is that multi-power- conversion units are used to achieve high voltage gain, which is reduced the converter reliability. A novel single-input-dual output impedance network converter is presented in [12]. The disadvantage of the designed converters is that the DC-Link capacitors are suffered from high voltage gain in addition to the reduction of the converter reliability because of the decreasing in the DC-Link capacitors life cycle. A single-phase impedance source inverters are introduced in [13]. The presented topologies with high frequency transformer have lower voltage gain compared to Y-source-based inverters. A new magnetically coupled Z-source impedance networks was proposed in [14]. The proposed topology discussed how to reduce the saturation problem of the Y-impedance core. In [15]–[24], single Y-source impedance network converters were presented to achieve high voltage gain for power inverters with continuous and/or discontinues input current capability. A new HB DC-DC converter for wide range input voltage applications was presented in [25]. High duty cycle ratio is used (expanded to 100%) to achieve only twice the voltage gain of the conventional HB inverter. On the other side, HB inverters with Y-source networks can achieve way higher than twice the voltage gain of the traditional HB inverters with the same number of active circuit components.

This paper presents a one stage DC-AC conversion unit with a simple control method, low voltage stress across the components, and a wide variety of output voltage level with extra voltage gain – based double Y HB inverter. It is very useful for renewable energy application and especially photovoltaic systems. Detailed information about the converter design and operation are described in the next sections. The rest of the paper is organized as follows. Section 2 represents inverter design and operation. The concept of the topology components selection is presented in 3. In section 4, simulation results are explored and discussed. The conclusion is finally given in section 5.

2. INVERTER DESIGN AND OPERATION

The proposed inverter, as shown in Figure 1, consists of double Y-impedance networks, switching devices, power diodes, input inductors, and capacitors. The main merits of using double-Y-source networks are to provide a neutral point for the load connected with no need to use DC-Link capacitors, higher voltage gain compared to using single Y-impedance, and to achieve symmetrical output AC voltage waveform. Small cores can be used for the Y-inductors to achieve high enough voltage gain; compared to using a single Y-impedance network. The three windings of each Y-impedance (L11, L21, L31, and L12, L22, L32) are wounded on a ferrite core. The input capacitors (Cin1, Cin2) have an important role in reducing core saturation problem by blocking the DC current component in the first winding (L1) of both Y-impedance networks. The Y-impedance capacitors (C11, C12) contribute to blocking the DC current component in the second winding (L2) of each Y-impedance network. Hence, symmetrical AC current flows through all the windings of the Y-impedance networks as shown in the operating principles of the topology in next. In so doing that, the saturation problem of the Y-impedance cores is addressed out.

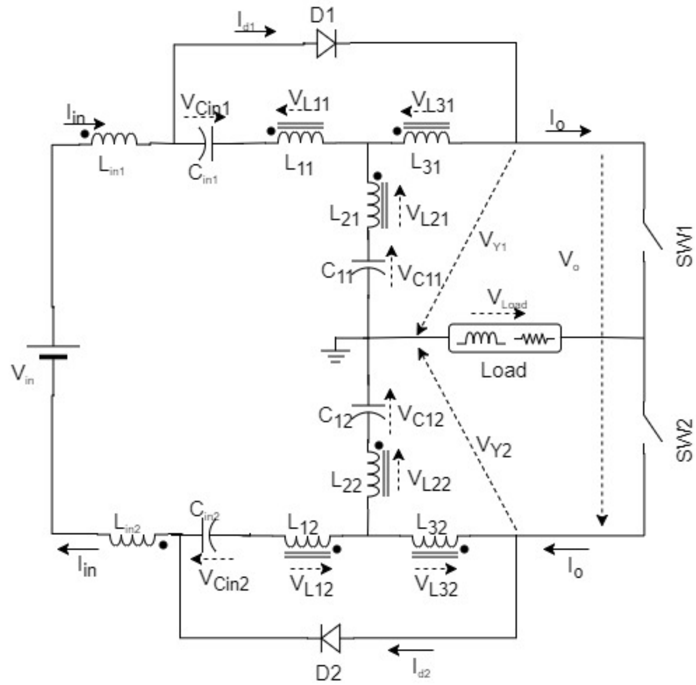

Figure 1. Proposed double Y-source symmetrical inverter topology

In order to achieve symmetrical output AC voltage, the two Y-impedance networks should have identical passive components. Therefore, each component in the first Y-network (Y_1) has an equal value to it's in the second Y-network (Y_2), where $L_{in1}=L_{in2}=L_{in}$, $C_{in1}=C_{in2}=C_{in}$, $L_{11}=L_{12}=L_1$, $L_{21}=L_{22}=L_2$, $L_{31}=L_{32}=L_3$, and $C_{12}=C_{11}=C$. The operation principles of the proposed converter are explained based on two operating states: (a) Non-Shoot-Through-State (NSTS) and (b) Shoot-Trough-State (STS). In the NSTS, only one of the switches (SW1, SW2) is ON; while the other one is OFF. In the STS, both switching devices are ON. The diodes (D1, D2) are only in off state when both switching devices are ON.

2.1 Non-shoot-through-state (NSTS)

In the NSTS, there are two operating states. The first one is when SW1 is ON, while SW2 is OFF, as shown in Figure 2 (a), a positive voltage appears across the load which is contributed by Y_1. The AC load voltage level is equal to the half gained voltage of Y_1 ($V_{Y1}/2$) as shown in Figure 3. The second operating state is that when SW2 is ON and SW1 is OFF, as shown in Figure 2 (b), in the opposite of the first operating state, a negative output AC voltage can be noted across the load in this state which is ($-V_{Y2}/2$). During this state, the Y-capacitors are charging up. Generally speaking, both diodes are only conducted during the NSTS. Using the loop voltage equations, the system equations for the NSTS are shown in below

$$V_{\text{in}} - 2V_{\text{Lin}} + 2V_{\text{Cin}} - 2V_L - 2a_{21}V_L - 2V_C = 0 \quad (1)$$
$$V_{\text{in}} - 2V_{\text{Lin}} - V_{\text{DC}} = 0 \quad (2)$$

by substituting equ. (2) in equ. (1), the output voltage of the Y-networks is

$$V_{\text{o}} = -2V_{\text{Cin}} + 2V_L + 2a_{21}V_L + 2V_C \quad (3)$$

$$-2a_{31}V_L - 2V_L + 2V_{\text{Cin}} = 0 \quad (4)$$

where $a_{21} = \frac{N_2}{N_1}$, $a_{31} = \frac{N_3}{N_1}$, $V_{L1} = V_L$, $V_{L2} = a_{21}V_L$, and $V_{L3} = a_{31}V_L$

2.2 Shoot-through-state (STS)

Both switches (SW1 & SW2) are ON in this state, as shown in Figure 2(c), while both diodes are in reverse blocking operation mode (OFF state). The output voltage of both Y-networks (V_o) is zero; so zero AC voltage appears across the load as shown in Figure 3. During the STS, the energy is being released from the capacitors and stored in the Y-inductors to achieve high voltage gain during the NSTS. With increasing the STS duration (t_s or D_S), more energy would be stored in the Y-inductors which results in higher voltage gain. The loop voltage equations of the STS are described below

$$V_{\text{in}} - 2V_{\text{Lin}} + 2V_{\text{Cin}} - 2V_L - 2a_{21}V_L - 2V_C = 0 \quad (5)$$
$$-2a_{31}V_L + 2a_{21}V_L + 2V_C = 0 \quad (6)$$

By applying volt-second balance for the Y-inductor (L) using equ. (4) and equ. (6), the voltage of the capacitors is derived as follows

$$V_C = \frac{(1-D_S)(N_2-N_3)V_{\text{Cin}}}{D_S(N_1+N_3)} \quad (7)$$

By also applying volt-second balance for the input inductor (L_{in}) using equ. (1) and equ. (5), other capacitors voltage equations are derived as follows

$$V_C = \frac{1}{2}(2V_{\text{Cin}} + V_{\text{in}}) \quad (8)$$

From equ. (7) and equ. (8), the final capacitor voltage equations are derived as shown below

$$V_C = \frac{(1-D_S)V_O}{2} \quad (9)$$
$$V_{\text{Cin}} = \frac{D_S(M-1)(V_O)}{2} \quad (10)$$

By substituting equ. (4), equ. (9) and equ. (10) in equ. (3), the peak-peak output voltage (V_o) of the proposed topology is derived as follows

$$V_{\text{o}} = \frac{V_{\text{in}}}{1-MD_S} = G\,V_{\text{in}} \quad (11)$$

While in principle operation of the conventional HB inverter, the RMS load voltage is equal to

$$V_{\text{Load RMS}} = \frac{V_{\text{o RMS}}}{2} \quad (12)$$

where $= \frac{(N_1+N_2)}{(N_2-N_3)}$, and $G = \frac{1}{1-MD_S}$

The relationship between the peak-peak load voltage gain and the shoot-through duty cycle (D_s) is plotted for different (M) values, as shown in Figure 4. The plot shows that the shoot-through duty cycle (D_S) region is restricted by the selected M value.

In principles operation of buck-boost converters, traditional buck converter has a voltage gain (V_o/V_{in}) which is less than or equal to 1, while the boost converter has a voltage gain greater than 1. The proposed source-impedance network converter works as a boost converter with a wide variety of the output AC voltage level. It can be noticed from the gain curves, as shown in Figure 4, that there are two operation quarters: positive and negative boost operation quarters. For the positive boost operation region, the shoot-through duty cycle (D_S) is ($0.5 > D_s > 0$). In the negative boost operation region, the shoot-through duty cycle is ($1 > D_s > 0.5$).

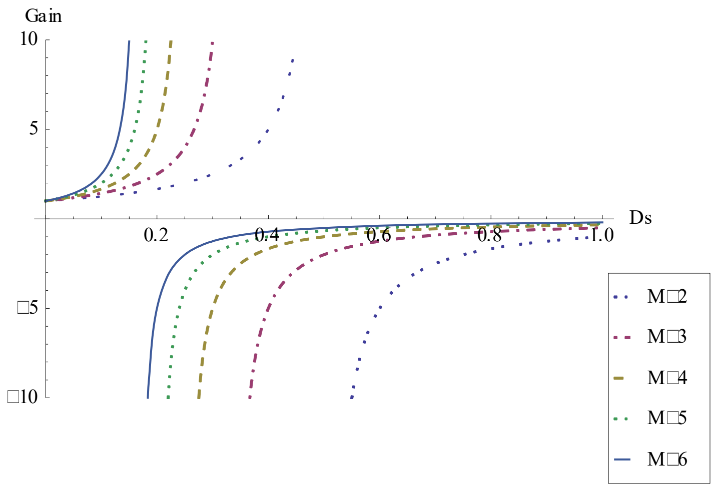

Figure 4. Possible voltage-gain for the proposed topology with respect to shoot-through duty cycle at different M values.

3. RESULTS AND DISCUSSION

The proposed topology is simulated in detailed using PSpice simulation tools. The simulation tests conditions are listed in Table 1, both Y-impedance networks components are identical. The simulation results verified the operational concept of the proposed topology and the derived equations. The gate voltage of the switching devices is shown in Figure 5(a). It shows that an overlapped pulse width modulation (PWM) strategy is used where the shoot-through occurs on both sides of the gate pulses. This simple overlapped method is used to achieve symmetrical output AC waveform instead of using single side overlapped PWM which results in asymmetrical AC output voltage. The gained voltage by both Y-impedance networks is shown in Figure 5(b). The first Y-network voltage is positive which is V_{Y1}, while the second Y-network voltage is negative which is V_{Y2}. The difference between both impedance networks (V_{Y2}-V_{Y1}) represents the load voltage (V_o) as shown in Figure 5(c). It can be noted that high voltage (V_o) is gained from 24 V input voltage.

Table 1 Simulation circuit conditions.

Parameter / description	Value	Parameter / description	Value
Power rating	72 W	Input capacitor (C_{in})	50 µF
Input voltage (V_{in})	24 volt	Y- coupled inductors (L_1, L_2, L_3)	288 µH, 800 µH, 32 µH
RMS Y-networks output voltage (V_o)	320 volt	Y-capacitors (C_1)	50 µF
RMS load voltage (V_{Load})	160 volt	Y-impedance cores	Ferrite Core
Peak-peak load voltage ($V_{Load\ p\text{-}p}$)	442 volt	Y-impedance windings factor (M)	2
RMS Y-networks output current (I_o)	9.3 A	R-Load	350 Ω
RMS load current (I_{Load})	0.45 A	Switching frequency	20 kHz
Input inductor (L_{in})	288 µH	Shoot-through duty cycle (D_s)	47.3%
Diodes (D1 & D2)	High voltage blocking capability	Switching devices (SW1 &SW2)	High voltage blocking capability

Both diodes share the same amount of voltage stress as shown in Figure 6(b). The small oscillation in the diode's voltage represents the parasitic elements of the simulation circuit. Almost an equal voltage stress across the input capacitors and Y-networks capacitors are shown in Figure 6(c) and Figure 6(d), respectively. The simulation current results are shown in Figure 7. The input current, as shown in Figure 7(a), is continuous current. The diode and switching devices currents are shown in Figure 7(b) and Figure 7(c), respectively. The load current is shown in Figure 7(d) based on a resistive load. The Y-network currents (i_{L1}, i_{L2}, and i_{L3}) are shown in Figure 8(a), Figure8 (b), and Figure 8(c). It can be noted that they are symmetrical around the x-axis which has a significant role in preventing the Y-cores from the saturation.

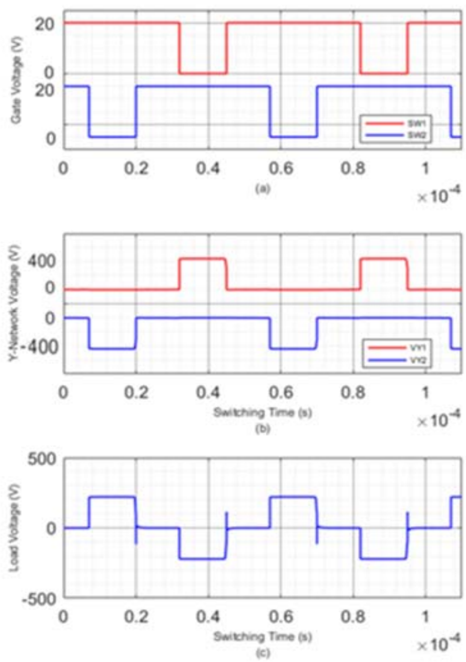

Figure 5. Simulation results of the proposed converter: (a) Swhitches gate voltage, (b) Output voltage eah Y-impedance network, (c) Load voltage

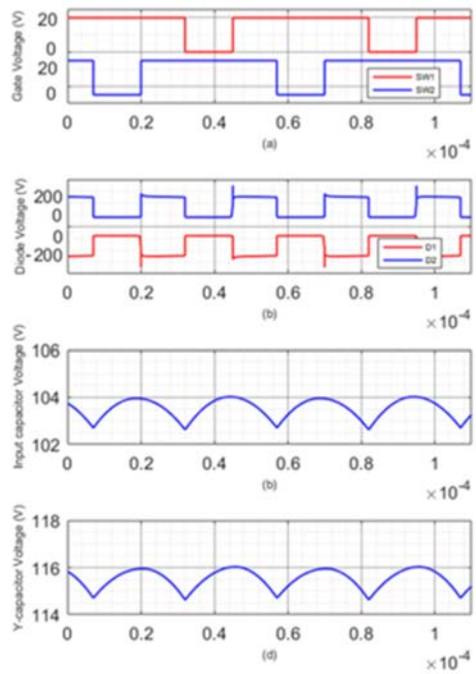

Figure 6. Simulation results of proposed converter: (a) Switches gate voltage, (b) Diodes voltage, (c) Input capacitors voltage, (d) Y-capacitors voltage

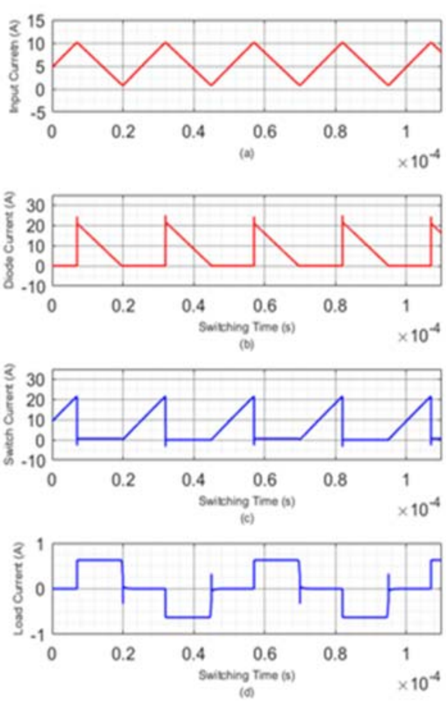

Figure 7. Simulation results of the proposed converter: (a) Input current, (b) diode (D1), (c) switching device (SW1) current, (d) load current

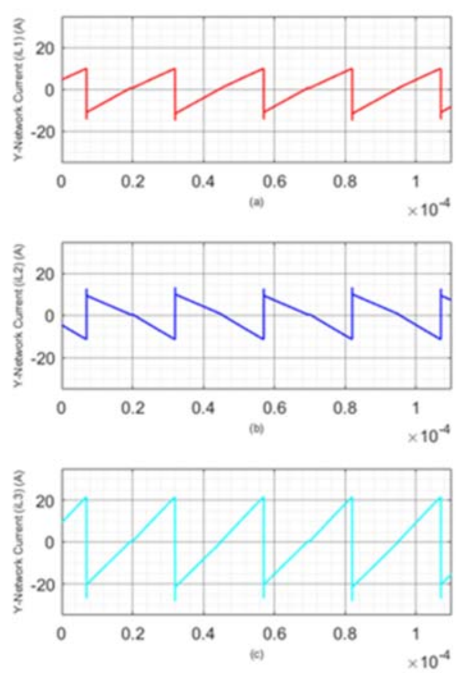

Figure 8. Simulation results of the proposed converter: (a) current of the first winding of Y-network, (b) current of the second winding of Y-network, (c) current of the third winding of Y-network

4. CONCLUSION

One stage high voltage half-bridge inverter is designed and analyzed using double Y-source networks. The simulation results show promising features for renewable energy applications such as high voltage gain, low voltage stress across the circuit elements, continuous input current, and symmetrical current waveforms in all Y-inductors which helps to prevent the Y-cores saturation. The other most important features of the HB converter are symmetrical AC load voltage and an inherited virtual neutral point for the load connection. The operation principles are discussed and studied deeply in this paper based on derived the formulas. The circuit components are selected based on mathematical equations for better power inverter design. Furthermore, PSpice simulation tools are used to validate the proposed converter operation modes and detailed derived mathematical formulas.

REFERENCES

[1] M. S. Pilehvar and M. Mardaneh, "Phase-shift control and harmonics elimination for H-bridge Z-source inverter," *IET Power Electron.*, vol. 8, no. 4, pp. 618–627, 2015.

[2] M. Nguyen, G. Cho, and Y. Lim, "Switched-Boost Network Based Single-Phase Boost DC-AC Converter," *IET Power Electron.*, vol. 9, no. 14, pp. 2723–2730, 2016.

[3] D. Vinnikov, A. Chub, and L. Liivik, "Asymmetrical Quasi-Z-Source Half-Bridge DC-DC Converters," in *9th International Conference on Compatibility and Power Electronics (CPE)*, 2015, pp. 369–372.

[4] Y. Zhao, X. Xiang, C. Li, Y. Gu, W. Li, and X. He, "Single Phase High Step-up Converter with Improved Multiplier Cell Suitable for Half-Bridge Based PV Inverter System," *IEEE Trans. Power Electron.*, vol. 29, no. 6, 2014.

[5] D. Cao, S. Jiang, F. Z. Peng, and Y. Li, "Low Cost Transformer Isolated Boost Half-bridge Micro-inverter for Single-phase Grid-connected Photovoltaic System," in *Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2012, pp. 71–78.

[6] E. Babaei and E. S. Asl, "High-Voltage Gain Half-Bridge Z-Source Inverter With Low-Voltage Stress on Capacitors," *IEEE Trans. Ind. Appl.*, vol. 64, no. 1, pp. 191–197, 2016.

[7] E. Babaei, E. S. Asl, and M. H. Babayi, "Steady - State and Small - Signal Analysis of High Voltage Gain Half - Bridge Switched - Boost Inverter," *IEEE Trans. Power Electron.*, vol. 63, no. 6, pp. 3546–3553, 2016.

[8] D. Vinnikov, A. Chub, O. Husev, and J. Zakis, "Quasi-Z-Source Half-Bridge DC-DC Converter for Photovoltaic Applications," in *IEEE International Conference on Industrial Technology (ICIT)*, 2015, pp. 2935–2940.

[9] G. Zhang, Z. Li, B. Zhang, D. Qiu, W. Xiao, and W. A. Halang, "A Z-Source Half-Bridge Converter," *IEEE Trans. Ind. Electron.*, vol. 61, no. 3, pp. 1269–1279, 2014.

[10] E. Babaei and E. S. Asl, "High Voltage Gain Half - Bridge Z - Source Inverter with Low Voltage Stress on Capacitors," *IEEE Trans. Ind. Electron.*, vol. 64, no. 1, pp. 191–197, 2017.

[11] Y. Liu, H. Abu-rub, and B. Ge, "Front-End Isolated Quasi-Z-Source DC – DC Converter Modules in Series for High-Power Photovoltaic Systems — Part I : Configuration , Operation , and Evaluation," *IEEE Trans. Ind. Electron.*, vol. 64, no. 1, pp. 347–358, 2017.

[12] G. Zhang, B. Zhang, Z. Li, Y. Zhang, and S. Chen, "A Novel Single-Input-Dual-Output Impedance Network Converter," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 6777, no. c, pp. 1–9, 2017.

[13] Z. Aleem, H. F. Ahmed, H. Cha, and H. G. Kim, "Single-phase isolated impedance-source inverters," *9th Int. Conf. Power Electron. - ECCE Asia "Green World with Power Electron. ICPE 2015-ECCE Asia*, pp. 129–134, 2015.

[14] Y. P. Siwakoti, F. Blaabjerg, and P. C. Loh, "New Magnetically Coupled Impedance (Z-) Source Networks," *IEEE Trans. Power Electron.*, vol. 31, no. 11, 2016.

[15] V. Behjat, S. Semko, and H. Nobahar, "Permanent-Magnet Synchronous Generator and Y Source Converter," in *The 6th Power Electronics, Drive Systems & Technologies Conference*, 2015, pp. 340–345.

[16] R. R. Ahrabi and M. R. Banaei, "Improved Y -source DC – AC converter with continuous input current," *IET Power Electron.*, vol. 9, no. 4, pp. 801–808, 2016.

[17] M. Forouzesh and A. Baghramian, "Galvanically isolated high gain Y-source DC – DC converters for dispersed power generation," *IET Power Electron.*, vol. 9, no. 6, pp. 1192–1203, 2016.

[18] Y. P. Siwakoti, F. Blaabjerg, and P. C. Loh, "Quasi Y-Source Boost DC-DC Converter," in *European Conference on Power Electronics and Applications*, 2015, vol. 8993, no. c.

[19] Y. P. Siwakoti, P. C. Loh, F. Blaabjerg, S. J. Andreasen, and G. E. Town, "Y - Source Boost DC / DC Converter for Distributed Generation," *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 1059–1069, 2014.

[20] Wang, Yijie, Wenli Jing, Yuping Qiu, Yuanyuan Wang, Xiangyuan Deng, Ke Hua, Benran Hu, and Dianguo Xu. "A family of Y-source DC/DC converter based on switched inductor." *IEEE Transactions on Industry Applications* 55, no. 2, pp. 1587-1597, 2018.

[21] Ji, Yuliang, Hongchen Liu, Feng Yong, Fengjiang Wu, and Pat Wheeler. "High Step-Up Y-source Coupled-Inductor Impedance Network Boost DC-DC Converters with Common Ground and Continuous Input Current." *IEEE Journal of Emerging and Selected Topics in Power Electronic*s, 2019.

[22] Reddivari, Reddiprasad, and Debashisha Jena. "Novel active clamped Y-source network for improved voltage boosting." *IET Power Electronics*, vol. 12, no. 8, pp. 2005-2014.

[23] Chen, Manxin, Changqing Yin, and Poh Chiang Loh. "Magnetically-Coupled High-Voltage-Boost Split Y-Source Inverter without Leakage-Induced Voltage Spikes." I*EEE Transactions on Industrial Electronics*, 2019.

[24] Zhang, Neng, Guidong Zhang, and Khay Wai See. "A Δ-Y Hybrid Impedance Network Boost Converter With Reduced Input Current Ripple." *IEEE Transactions on Power Electronics*, Vol 33, no. 4, pp. 2803-2808, 2017.

[25] H. Jang, T. Ahn, and B. Choi, "New half-bridge dc-to-dc converters for wide input voltage applications," in *31st International Telecommunications Energy Conference*, 2009.

BIOGRAPHIES OF AUTHORS

Hussain Sayed has gained his master's degree of science in Systems Engineering from the University of Arkansas at Little Rock - USA, in 2016. His bachelor's of science degree was awarded from the University of Technology – Baghdad, Iraq, in 2010. Mr. Sayed has been working on investigating WBG devices and in particular SiC power switching devices performance for over four years. He also works on designing high-voltage gain power electronics converters for renewable energy applications. He has published several papers in IEEE proceedings in the U.S. and Canada, in addition to accredited international journal publications. Mr. Sayed has strong theoretical and experimental experiences in using LabVIEW software and equipment in both academia and industrial sectors. Hussain's roles as an active reviewer in IEEE and Springers journals.

Oday A. Ahmed received his MSc degree in Electrical and Electronic Engineering from University of Technology, Baghdad-Iraq, in 2002. He was awarded a PhD degree from University of Leicester in 2012. Since 2002, he has been a Lecturer in Electrical Engineering in the Department of Engineering at the University of Technology, where he teaches Electrical Machines, Power Systems and power electronics. His field of research covers a wide range of subjects in Renewable Energy Conversion and Energy Storage, from electrical generators and power electronics to power systems and advanced controllers.

Dhari Y. Mahmood is an asst. Prof at the at the Department of Electrical Engineering at the University of Technology, Iraq. He is currentaly, the dean of the Department of Electrical Engineering. He has gained jis M.Sc and PhD in Electrical Power Engineering from Sant. Peterburg polytechnical Institute-Russa in 1986 and 1990 respectively. His BSc degree received in 1981 from University of Baghdad-Collage of Engineering -Iraq. Hw wok in the field of renewable energy and power system research. He supervises a large number of graduate students in both master's and Ph.D. degrees.

Kanaan A. Jalal is a Lecturer at the Department of Electrical Engineering at the University of Technology, Iraq. He received his Ph.D. in 2007 at University ofTechnology, Iraq. His research interests include electrical power engineering, renewable energy, and the application of soft computing techniques on different power system problems.

Waleed H. Habeeb is a Lecturer at the Department of Electrical Engineering at the University of Technology, Iraq. He received his M.Sc.. in 1985 at University of Technology, Iraq. His research interests include power electronics, renewable energy , energy efficiency engineering, and cathodic protection systems .